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SELECTED AREA EPITAXIAL GROWTH FOR COMPLEMENTARY HBT APPLICATIONS

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Attn: Dr. James W. Mink
Director, Electronics Division

Prepared by:

C. W. Farley

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This report describes the development of a complementary AlGaAs/GaAs heterojunction bipolar transistor (HBT) technology with a highly merged process that simplifies device fabrication without altering or compromising device design. Selected area molecular beam epitaxy (MBE) was used to monolithically integrate Npn and Pnp devices. These devices show performance levels comparable to separately processed devices. For the first time, microwave frequency integrated circuits were fabricated from both types of devices on the same wafer.

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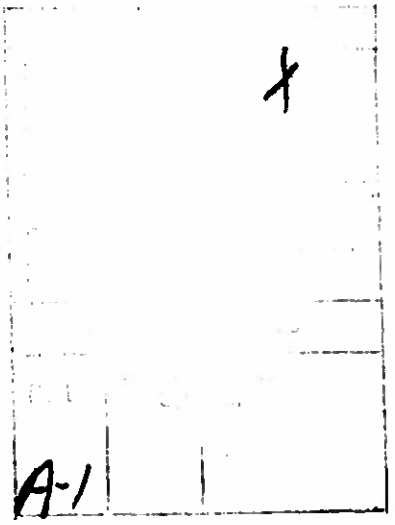
A digital mask set and the Rockwell baseline digital HBT process were modified to develop a merged process. This process includes the use of a light field emitter to provide passivation which reduces surface recombination at the base-emitter junction. This is the first time that edge passivation, which results in increased gain in Npn devices, has been demonstrated to increase gain in Pnp structures. The merged digital process was designed to maximize the number of steps in which both devices could be processed simultaneously, and the resulting process has only two more mask levels (Pnp base and collector metallization) than the baseline process.

Monolithically integrated devices with 1.4 μm x 12 μm emitters show performance levels equal to values typical for separately processed Npn and Pnp transistors. Pnp devices exhibit f_T = 20 GHz and f_{max} = 19 GHz at I_c = - 5.5 mA and V_{ce} = -2 V. Npn devices show f_T = 51 GHz and f_{max} = 60 GHz at i_c = 12 mA and V_{ce} = 1.5 V.

For the first time, microwave frequency integrated circuits were fabricated from both types of devices on the same wafer using the merged process. Npn-based direct coupled feedback amplifiers show a gain of 11 dB and a bandwidth of 12 GHz. In the first demonstration of a Pnp-based HBT integrated circuit, Pnp-based gain blocks show gain of 8 dB and a bandwidth of 6 GHz. Pnp performance limitations were analyzed, revealing the potential for significant improvement in Pnp performance through reduction in emitter resistance, optimization of the collector layer structure, and higher base doping. Improved device performance should result in improved circuit performance. For Npn and Pnp HBT-based gain blocks, circuit bandwidth is proportional to ~0.3 * f_{max}, demonstrating that Pnp devices can be simply introduced into direct coupled circuit topologies without significant speed penalties, and that improvements in f_{max} will result in higher circuit operating bandwidths.



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I. STATEMENT OF THE PROBLEM STUDIED

This is the final report for contract number DAAL 03-89-C-0014 entitled "Selected Area Epitaxial Growth for Complementary HBT Applications," which covered the period 5/1/89 through 4/30/92.

High performance electronic devices are key to the success of many advanced DoD systems. For example, future communication and radar systems will require transistors that operate into the millimeter-wave region with high power added efficiency. In addition, advanced high speed digital signal processing applications will require higher integration levels than are now attainable. These goals must be met in light of an increasing demand for highly portable, light weight communication systems. These constraints raise the importance of low static power dissipation significantly, and represent one of the major motivations for research on complementary heterojunction bipolar transistors (HBTs)

Heterostructure devices based on the AlGaAs materials system have achieved impressive device and circuit performance at the Rockwell International Science Center. Baseline digital Npn AlGaAs HBTs fabricated by using conventional optical lithography and 1μm or larger design rules have routinely exhibited gain of 100 with cutoff frequency (f_t) and maximum oscillation frequency (f_{max}) of ~55 GHz. Many high-performance digital and analog circuits have been realized with the Rockwell baseline HBT technology. We have demonstrated (jointly with Bellcore) a 30 Gb/s 2:1 mux, a 27 Gb/s 1:2 demux, a 27 Gb/s 4-bit mux/demux, a 7 Gb/s 8-bit mux/demux and a 20 Gb/s decision circuit.[1-2] 8 GHz 1000-gate arrays and 15 GHz 500-gate arrays were also realized (jointly developed with IBM).[3-4] Various frequency dividers have been fabricated and operated up to 25 GHz.[5] We are developing high performance ADCs (6 GHz 6-bit and 1.5 GHz 8-bit) and DAC (1.2 GHz 12-bit) with the HBT technology. The very promising performance of these integrated circuits has resulted in transfer of the baseline Npn AlGaAs HBT technology to Rockwell's Compound Semiconductor Products manufacturing facility.

The most significant performance limitation of HBT devices and circuits to date is related to power dissipation. This is a central issue with most, if not all, semiconductor technologies. The HBT technology offers improvement in microwave power-added efficiency, and in digital circuit power-delay product over competing high speed technologies, but further improvement is needed for widespread technology application. The impact of low power dissipation on performance of electronic systems is strongest because of its effect on level of integration. It is difficult to remove

heat from integrated circuits above a certain fixed amount (on the order of 3-5 W for air-cooled LSI, for example). This places a restriction on the number of gates/circuits that can be integrated on a chip. If the power dissipation per gate can be reduced, higher integration levels and reductions in overall system delay will be possible, since the time-consuming and power-intensive transmission of signals from chip to chip will be minimized.

A variety of strategies can be employed to reduce power consumption in integrated circuits. One of the most powerful is to use appropriate combinations of Npn and Pnp devices (complementary circuits). The output currents of the two device types respond to input voltages with transconductances of opposite sign. This allows turning off the current in one device while turning on the current in the other in a straightforward manner, a feature which can be applied in many different circuit contexts to achieve reduction of power consumption.

As examples of the benefits to be gained from the successful development of complementary HBT circuits we describe applications in microwave amplifiers, broadband analog circuits and digital circuits. Power amplification in the microwave regime is a widespread system requirement, and power-added efficiency of amplifiers is often the most critical amplifier specification. Class A amplifiers are restricted theoretically to at most 50% power-added efficiency, and in practice do not achieve more than 35%. Class B and C amplifiers, in which devices are switched off for 50% or more of the rf cycle, can achieve in principle 79% and 100% power-added efficiency, respectively. As a result of their nonlinear operation, however, harmonics of the input frequency are generated in such amplifiers. The most efficient approach, demonstrated during years of Si bipolar amplifier development, is to use pairs of transistors biased in Class B or C arranged in push-pull fashion. Even harmonics are thereby eliminated from the output. Simple, broadband input signal circuitry, biasing circuitry, and output power-combining circuitry result from the use of Npn/Pnp combinations.

Operational amplifiers, variable gain amplifiers, comparators and analog/digital converters can also benefit from complementary Npn/Pnp combinations in several areas. Pnp transistors provide active loads, enabling high incremental load resistance (and thus high voltage gain) without the voltage drop and power dissipation that would be required from resistive loads. In addition, complementary transistors are used in push-pull output drivers. As in the case of microwave amplifiers, the transistors operate in class B, and the arrangement provides significant power savings over conventional circuits. Unlike the microwave case, the transistors are used in a common collector configuration (as emitter followers), providing very low output impedance. This mode of operation is unattractive at very high (microwave and mmwave) frequencies because

of stability considerations, but is universally used in broadband, dc-coupled bipolar circuitry to date. A final application of Pnp/Npn devices, unrelated to power savings, is to compensate the input base current of amplifier transistors to allow ultrahigh input impedance (as needed, for example, in a sample-and-hold circuit).

Although in Silicon digital circuit technology, pnp transistors monolithically integrated with npns are presently slow lateral devices, pnps have been used to reduce power dissipation in I^2L circuits (where the pnps are merged with existing structures) and in static RAM circuits. There is a significant research effort underway to produce high f_t pnp devices in Si bipolar technology, to implement further circuit approaches to reduce power. Heterojunction bipolar transistor technology offers the possibility of even greater benefits from Pnp/Npn combinations, because: (a) the Npn and Pnp HBTs can have much higher f_t and f_{max} than in Silicon and (b) the Npn and Pnp HBTs can potentially be effective even if operated in saturation. With HBTs there are realistic prospects of achieving a bipolar analog of CMOS circuits, having very low static power dissipation. Since static power dissipation accounts for 50-90% of the total dissipation of logic circuits, the overall improvement is potentially very large. The resulting logic family may be expected to have speed greater than that of present Si ECL logic, with power dissipation nearly as low as CMOS. The system impact of such a logic family would be very large. The detailed circuit design of complementary HBT logic gates may take various forms. However, in general, the critical element for the complementary HBT logic (CHBTL) is the output driver pair, which has high current drive capability under transient conditions, and has very low static power dissipation (given by the power associated with output buffers).

To realize the circuit benefits outlined above, the Pnp and Npn transistors must satisfy a number of requirements: 1) High f_t and f_{max} is needed for all applications, particularly in microwave uses. 2) Current gain must be moderate for microwave and analog applications, and must be high for digital applications. 3) Matching of input characteristics of Npns and Pnps is beneficial (although not mandatory) in microwave circuits. 4) Very stringent requirements must be met for complementary HBT logic: in addition to being fast in normal mode operation, the devices must store little charge when operated in saturation mode, and the current gain must remain high in saturation mode. This last requirement is equivalent to the need for high current gain when operated in both the upward and downward directions (that is, in normal mode and with emitter and collector regions interchanged). We will refer to this requirement as "reversibility."

The program described in this final report was designed to study the development of a complementary AlGaAs/GaAs HBT technology that would address the problem areas and circuit

benefits outlined above. Two approaches (regrowth and overgrowth) for achieving monolithically integrated AlGaAs Npn and Pnp HBTs by selected area molecular beam epitaxy (MBE) were investigated. The simpler regrowth approach was highly successful and produced Npn and Pnp devices on the same wafer that define the state of the art in monolithic complementary HBT performance. A highly merged process was developed for this regrowth material that simplified device fabrication without altering or compromising device design. The more complex overgrowth approach yielded high resistivity materials that were not suitable for reversible transistor development. The most important results of the program are summarized in the next section.

II. SUMMARY OF IMPORTANT RESULTS

A. The Regrowth Process

The choice and development of a complementary HBT process is constrained by a number of considerations. The significance of such constraints and the process development which reflects these constraints is discussed here.

The first major concern is dopant migration during regrowth. At the impurity concentrations used in the base of the baseline Npn (4×10^{19} cm^{-3}), Be exhibits enhanced diffusion which is brought about by an increased interstitial Be population. For this reason, the growth of the Pnp structure is carried out first, so that the problem of controlling Be diffusion is restricted to the normal growth sequence of the Npn structure.

In order to produce selected area epitaxial growth so that the Npn devices could be located only where needed, appropriate regions of the Pnp device were protected with a dielectric during Npn regrowth

1. Choice of Dielectric

The process approach chosen calls for protecting regions of the Pnp with a dielectric so that an Npn layer structure can be grown on the wafer. The dielectric is then etched and the Pnp and Npn devices are processed. Concerns about Ga outdiffusion through SiO_2 led us to choose Si_3N_4 as the dielectric for initial experiments We experienced problems with the nitride cracking during regrowth, and modified this layer to be a composite dielectric of a 1500Å Si_3N_4 layer covered by a 2500Å silicon oxynitride layer. This dielectric survives regrowth, but like Si_3N_4, is difficult to remove in large areas. However, it can be easily removed from the small areas typically encountered in high speed devices and circuits.

2. Process for Easy Removal of Polycrystalline Deposit

The MBE regrowth of the Npn material produces a polycrystalline deposit on those regions of the wafer protected by the composite dielectric. Two approaches were tried for removing this polycrystalline overgrowth. The initial approach was to etch the dielectric, thereby lifting off the poly. With this approach it was difficult to etch under large areas (>100 μm) using reasonable dielectric thicknesses (<0.5 μm). We were able to reduce this problem by patterning the poly overgrowth, etching holes in it, and then etching the dielectric to lift the poly. Because these

results were only marginally satisfactory and the process was unnecessarily complicated, a different approach for the removal of the polycrystalline overgrowth was tried and successfully demonstrated. This process allows for complete removal of the overgrowth by etching, while the material from the original growth remains protected by the dielectric layer. The process sequence is outlined in Fig. 1. This process was successfully demonstrated on a 3-inch wafer, and was subsequently used for the regrowth approach to fabricate Pnp and Npn transistors on the same 3-inch wafer.

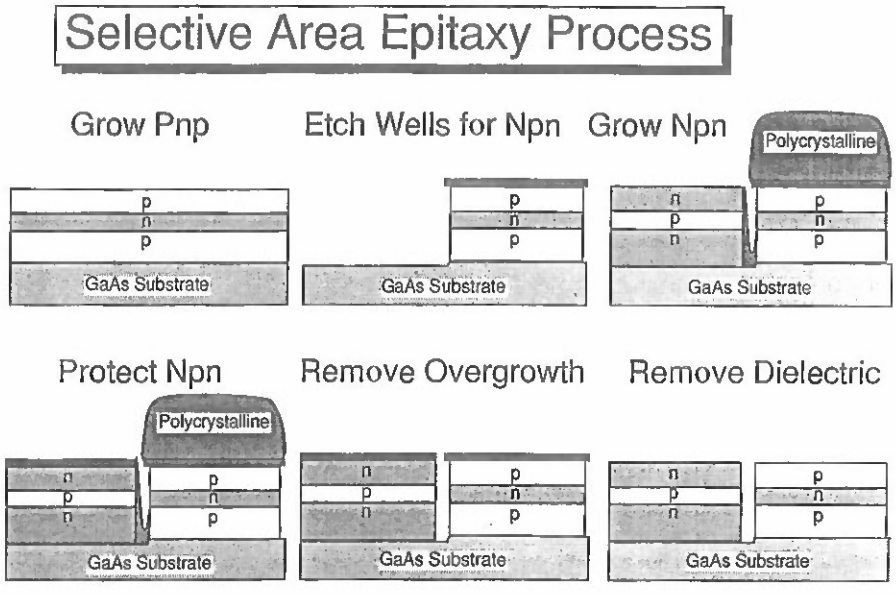


Fig. 1 Fabrication process developed for multiple selective area growths for complementary HBTs.

One critical measure of the complementary device fabrication process is the ability to make complementary ICs, which requires placing Npn and Pnp devices extremely close to one another (<10 μm). Our process for poly removal (Fig. 1) has produced results which satisfy this criteria easily, and suggest that Npn and Pnp devices may be placed within 5 μm of one another. Cross-sections of samples involving regrowth where the poly was removed using this process demonstrate excellent material quality very near the regrowth interface,and the surface near the edge of the regrowth interface shows excellent morphology. Figure 2 shows that there is a boundary region of about 5 μm outside of which smooth, high quality material is observed. Through the use of standard planarization techniques,[6] metal connections can be reliably made over these boundaries. The success of this technique for both negative- and positive-slope trenches is shown in Fig. 3.

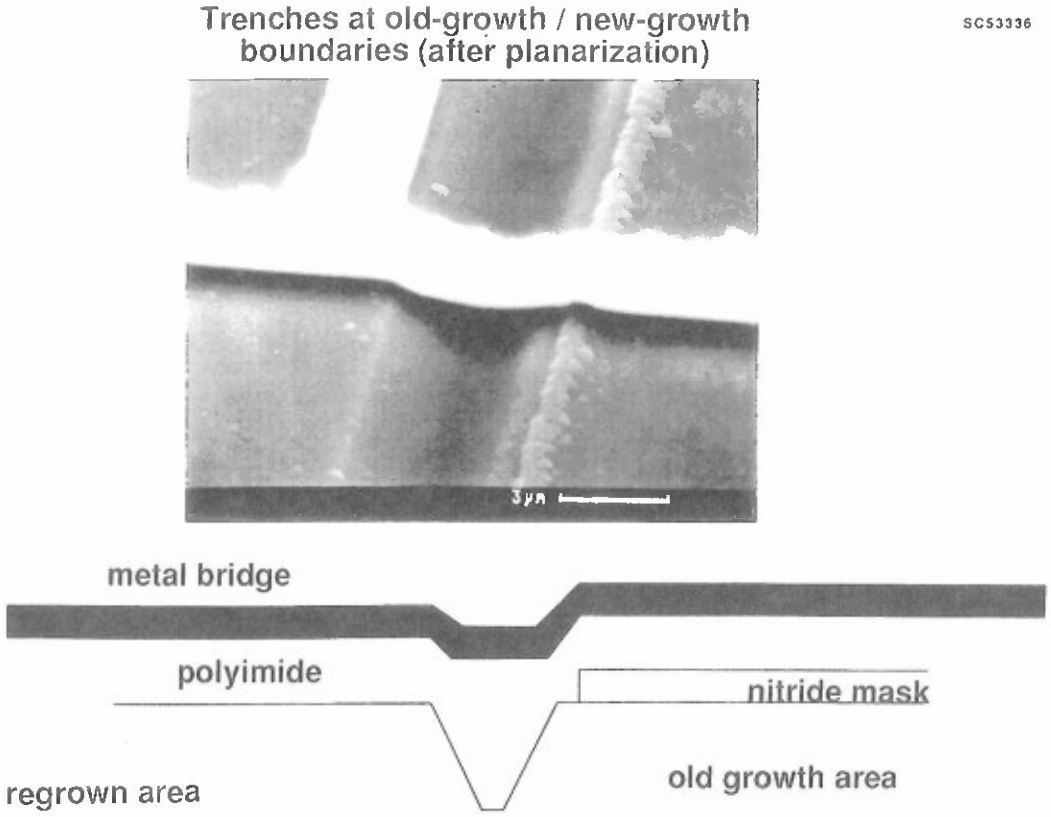


Fig. 2 Surface morphology near the regrowth boundary.

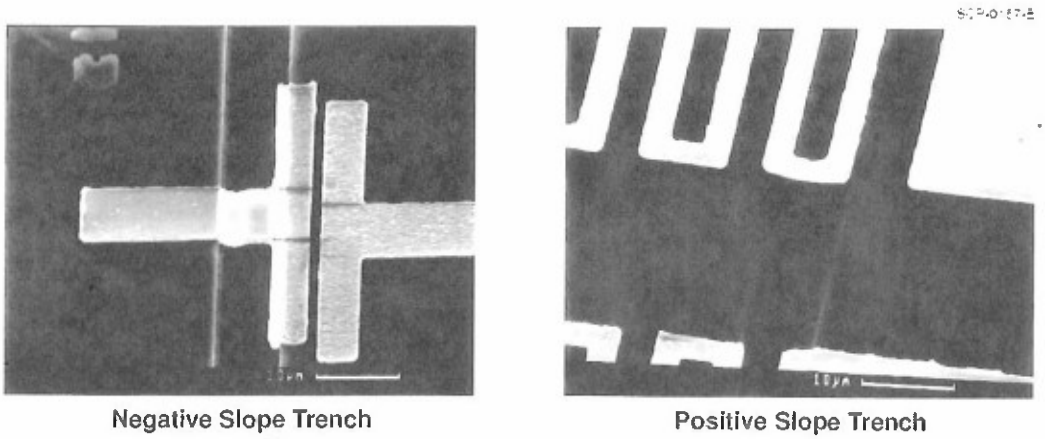


Fig. 3 Successful planarization across trenches with both negative and positive slopes.

B. The Overgrowth Process

To realize a reversible HBT it is necessary to fabricate transistors with equal emitter/base and base/collector junction areas. This requires an overgrowth process where the base layer is

overgrown on a dielectric in order to establish base contact. The overgrowth layer must be of adequate material quality to fabricate a low resistance contact. We investigated this key issue by simulating growth of Npn base layers on SiO_2. The GaAs layers were 700Å thick doped p-type to 2×10^{19} cm^{-3}. These samples showed high resistivity (~1×10^6 Ωcm) for growth temperatures ranging from 500 to 600°C, suitable for HBT growth. Some of the layers were subjected to additional thermal processing (rapid thermal anneals at temperatures from 400 to 700°C with GaAs proximity caps) in an attempt to lower resistivity by promoting growth of polycrystalline grain size. The results were uniformly disappointing, and the layers either remained unchanged or degraded. Because of these results, and the lack of progress at other laboratories in growing device quality GaAs on $SrCaF_2$, we chose to focus solely on the complementary regrowth process and device structure development.

C. Demonstration of Large Area Devices on the Same Wafer

As shown in Fig. 4, we have successfully demonstrated working Npn and Pnp devices monolithically integrated on a single wafer. The Pnp transistors were grown first, regions of the wafer were protected while these layers were removed in selected areas, and then Npn transistor layers were grown in these areas. The devices shown in Fig. 4 were independently processed into working HBTs. The Pnp transistor showed relatively low gain (~10). The Npn transistor showed extremely high gain (>200), reflecting the high quality of material in the regrown area. These devices were fabricated from large patterned areas, separated by ~1mm.

The low gain in the Pnp devices was initially attributed to Be diffusion during regrowth. However, when Pnp layers which had not been subjected to regrowth were processed, these layers also demonstrated low gain (Fig. 5a), and no effect of thermal cycling (which simulated the regrowth process) on device characteristics was observed (Fig. 5b). Measurements of base contact and sheet resistance indicated that the free electron concentration was lower than expected or desired, and was largely the cause of poor device performance. The Si doping level used in the base of the Pnp layers was very high (~7×10^{18} cm^{-3}), and at this level, the free carrier concentration is known to drop dramatically as growth temperature increases. It is likely that the resulting electron concentration was significantly less than intended.

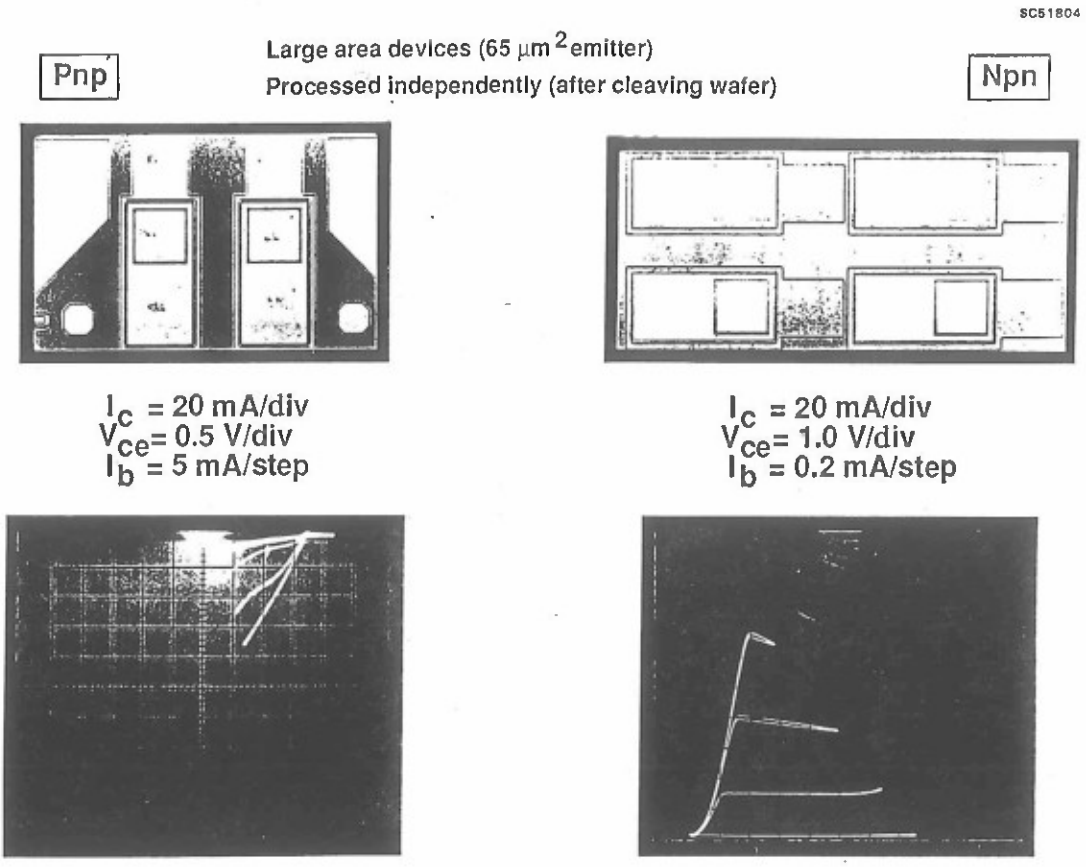
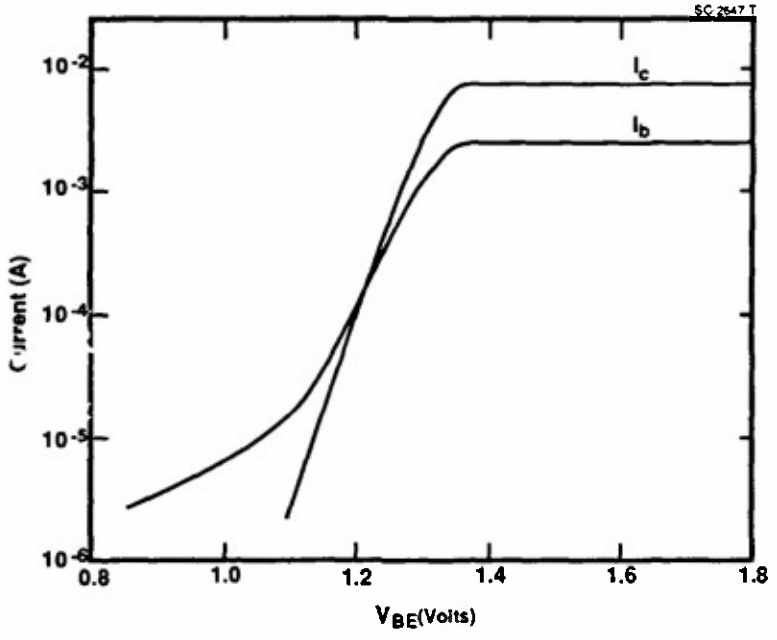


Fig. 4 Device layouts and I-V characteristics for Npn and Pnp HBTs separately processed from the same wafer.

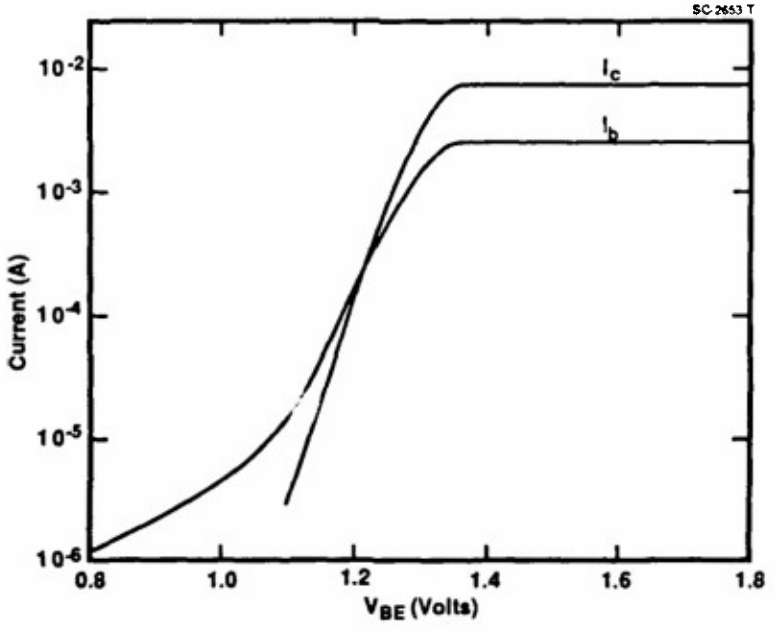
D. Optimization of the Pnp Transistor and Regrowth Process

In order to better understand the nature of the low Pnp gain and to improve this gain, we carried out a number of growths to determine a device structure which would give reproducible, high gain, with a high degree of uniformity in device characteristics. We observed that the gain drops as the Si base doping level increases. This effect is attributed to band filling in the GaAs base, which lowers the barrier to electron injection into the emitter, and raises the base current at a given base-emitter bias voltage. We have developed a device structure which gives reproducible device characteristics and which shows low frequency small signal gain in excess of 30. This structure is shown Fig. 6. Also shown in this figure is the baseline Npn structure which was used for all device results. The compositional grading at the base-emitter junction of both the Npn and Pnp layers was accomplished by continuously increasing the Al flux during the growth of this region. The Al flux was held constant during the growth of the constant composition section of the

emitter layer, and then continuously decreased to produce a smooth compositional change, returning to heavily doped GaAs.



(a)



(b)

Fig. 5 (a) Gummel plot of Pnp before thermal cycling; (b) Gummel plot of Pnp after thermal cycling.

Npn device structure

Contact	InGaAs	$n=1 \times 10^{20}$	600Å
n^+ Cap	GaAs	$n=1 \times 10^{18}$	1000Å
Emitter	AlGaAs	$n=5 \times 10^{17}$	950Å
Base	GaAs	$p=4 \times 10^{19}$	800Å
Collector	GaAs	$n=3 \times 10^{16}$	3000Å
Collector	GaAs	$n=6 \times 10^{16}$	4000Å
Subcollector	GaAs	$n=6 \times 10^{18}$	6000Å
Substrate	GaAs	undoped	25 mils

Pnp device structure

Contact	GaAs	$p=5 \times 10^{19}$	500Å
P^+ Cap	GaAs	$p=1 \times 10^{19}$	1000Å
Emitter	AlGaAs	$p=5 \times 10^{17}$	950Å
Base	GaAs	$n=1\text{-}4 \times 10^{18}$	800Å
Collector	GaAs	$p=4 \times 10^{16}$	4000Å
Subcollector	GaAs	$p=4 \times 10^{19}$	8000Å

Fig. 6 Schematic layer structure of Npn and Pnp devices.

The details of the regrowth process are now discussed in detail. The Pnp HBT was first grown on a 3-inch (100) GaAs wafer which had been spin etched for ~30 sec with a solution of 10:1:1 H_2O:NH_4OH:H_2O_2. This pretreatment has been shown to remove ~1 μm of material from the surface, an amount adequate to remove any surface layer containing residual polishing damage. Following thermal desorption of the surface oxide layer in the growth chamber in which a maximum temperature of 630°C was reached, as measured by an Ircon Series V pyrometer, the Pnp layer structures were grown at temperatures ranging from 580°C to 620°C. No significant dependence of device characteristics on growth temperature was observed.

The wafer was then removed from the vacuum system, and the composite nitride/oxynitride film was deposited over the wafer. This dielectric protection layer was patterned to protect the Pnp layers in areas where devices were to be fabricated, and to open regions for etching of wells for subsequent growth of Npn device layers. The depth of these wells relative to the top of the Pnp layer was chosen to match the thickness of the Npn layer, so that emitter contact metallizations would be coplanar. Following a 5 min. DI water rinse, the wafer was reinserted into the MBE system and, after thermal oxide desorption, the Npn layers were grown at a substrate temperature of 610°C for the subcollector and collector layers, and at temperatures ranging from 560 to 600°C for the base and emitter layers. Over this range, device characteristics vary systematically, with Npn gain being lowest at the lowest temperatures, and increasing monotonically with temperature, as a result of the reduction of mid-gap states in the AlGaAs emitter at higher growth temperatures. In addition, Be diffusion was negligible at 560°C, but as temperatures approached 600°C, noticeable Be diffusion into the emitter was indicated by an increase in the turn-on voltage of the base-emitter junction. Therefore, growth of an optimal Npn layer consisted of a tradeoff between

gain and turn-on voltage, one which was not severe for the base doping level used here (4×10^{19} cm^{-3}).

For the growth of the 600Å GaInAs/InAs contact layer for the Npn HBT, The In flux was kept constant at a growth rate of 0.25 monolayers/sec, while the Ga flux was decreased in four increments, so that a 300Å GaInAs grading region was composed of four sections of intermediate compositions which were each 75Å thick. The growth temperature was also decreased in a stepwise manner during the growth of these layers, so that a temperature of 400°C was reached by the time the growth of the 300Å InAs contact layer was begun. In order to produce smooth surface morphology, the As shutter was periodically opened and closed, reducing the time averaged As flux to one fourth of that used for the growth of the rest of the HBT.

In regions where the dielectric layer protected the Pnp layer, polycrystalline growth was observed in all cases. Following removal from the MBE system, a nitride/oxynitride layer was deposited over the areas of the wafer where single crystal Npn HBT layers were grown (the polarity of the mask used to pattern the dielectric protecting the Pnp layers during regrowth was inverted). The poly overgrowth was then removed using 1:1:6 $NH_4OH:H_2O_2:H_2O$, and the protecting dielectric layers were removed over the full wafer using buffered oxide etch (10 parts of saturated NH_4F solution to 1 part of HF). This process (described in the next section) produced side-by-side Npn and Pnp devices, with coplanar emitter contact layers.

E. Merged Process for Small Area Devices

Although large area devices can demonstrate the feasibility of a complementary process, the full evaluation of the process and relative device performance can only come from small area, high speed devices.

A suitable mask set was selected to develop the merged process. Key factors in the decision were the fabrication of a number of different size devices, as well as the realization of some simple circuits. For these reasons, and because of the process reliability, a digital mask set and the Rockwell baseline digital HBT process were chosen. This process includes the use of a light field emitter to provide passivation which reduces surface recombination at the base-emitter junction. This is the first time that the edge passivation process, which results in increased gain in Npn devices, has been demonstrated on Pnp structures.

Npn and Pnp devices were processed in separate fields (8.4mm x 8.4mm) in order to simplify fabrication. This approach, however, also produced a complication in retaining alignment

marks. Because some boundary regions near the alignment marks were etched during the removal of both the Npn poly regrowth over the alignment marks and the regrowth over the Pnp fields, trenches at these boundaries were especially wide and deep, which produced distortion in the photoresist, and reduced contrast for the step and repeat mask aligner. To minimize this problem, separate alignment marks were placed away from these boundaries, to obtain reliable alignment. This issue would not present a problem in the fabrication of complementary circuits, where the boundaries between Npn and Pnp devices will be well removed from the alignment marks.

Only a few modifications in the baseline digital Npn HBT fabrication process[6] were necessary to accommodate the concurrent processing of Npn and Pnp devices. At the base pedestal and light field emitter steps, etch processes were modified to cause the InAs/InGaAs contact layers of the Npn devices to be etched at near the same rate as the GaAs contact layers in the Pnp devices (40:2:1 H_2O:H_3PO_4:H_2O_2 was used). At the collector isolation implant step, the implant dose chosen as a result of isolation experiments on n-type and p-type GaAs test layers (He^+, 190 keV, 2.5 x 10^{14} cm^{-2} and He+, 380 keV, 2.0 x 10^{14} cm^{-2}) was a compromise designed to produce 10MΩ/sq for both devices, compared to the 100MΩ/sq which results from the standard Npn collector isolation implant.

In addition, the merged digital process was designed to maximize the number of steps in which both devices could be processed simultaneously. We have demonstrated concurrent processing of both device types at base pedestal, light field emitter, isolation, first level metal/emitter contact, as well as resistor and dielectric opening layers. During the contact metallization steps where both device types could not be processed simultaneously, the stepper was programmed to pattern alternate fields as appropriate. The resulting process (for realization of complementary circuits) is very streamlined, and consists of the baseline Npn HBT process with two additional mask levels (Pnp base and collector metallization). This merged process is outlined in Fig. 7.

F. Device and Circuit Results

DC results on small (1.4 μm x 3 μm emitter) devices are exceptional. Npn devices show a maximum value of ß = 200 at I_c = 4 mA and V_{ce} = 1.3 V (Fig. 8). Pnp devices show a maximum value of ß = 140 at I_c = -2.5 mA and V_{ce} = -2.2 V (Fig. 9).

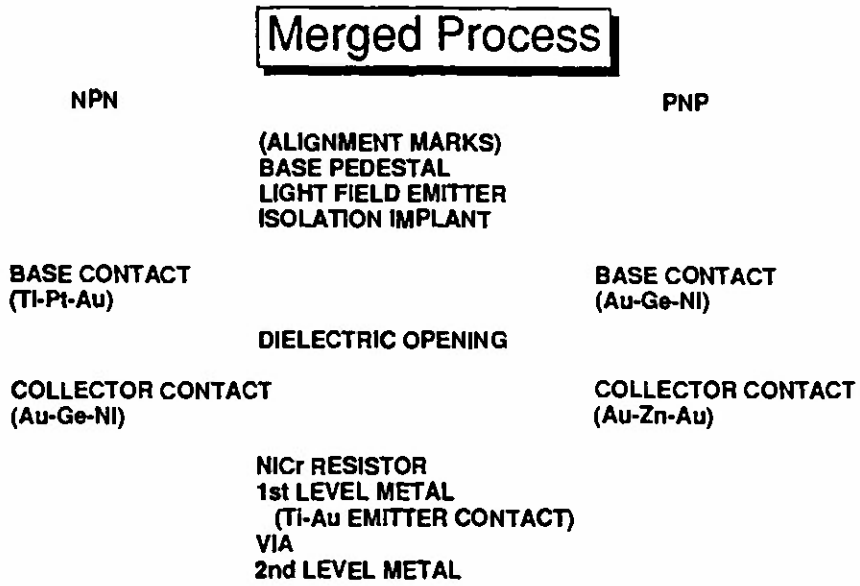


Fig. 7 Basic steps in the merged complementary HBT fabrication process.

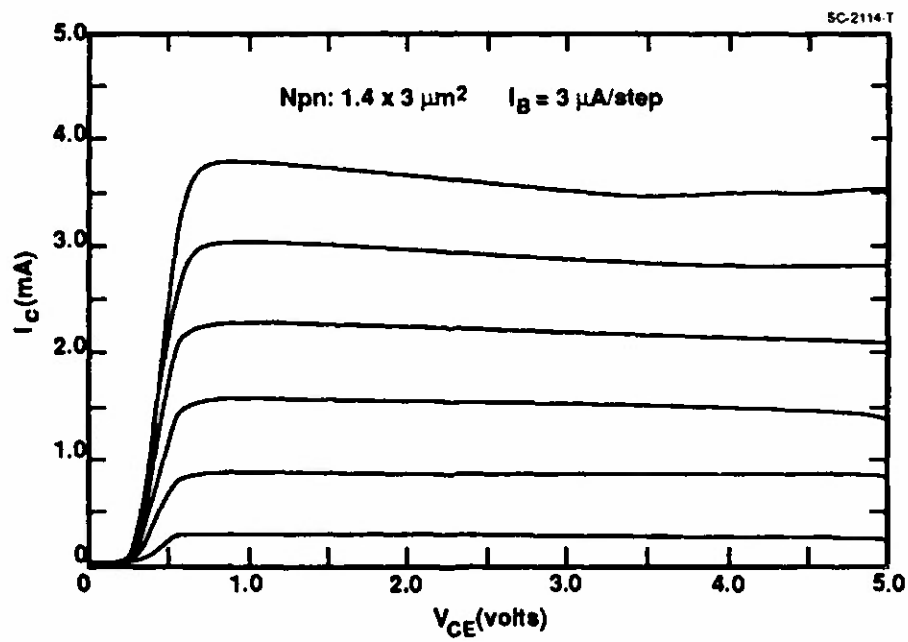


Fig. 8 I-V characteristics of a small area Npn device co-processed with Pnp HBTs using the merged process.

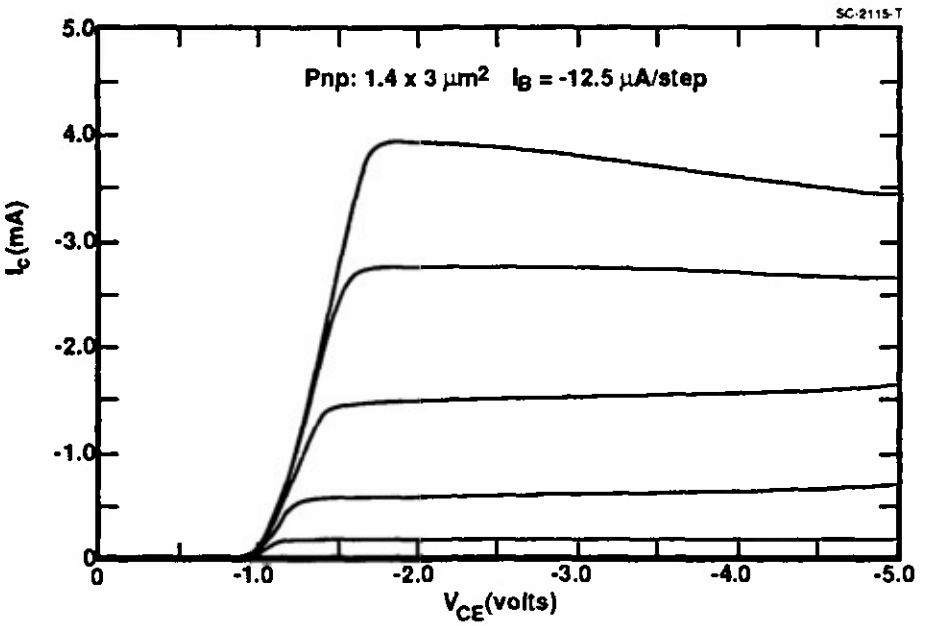


Fig. 9 I-V characteristics of a small area Pnp device co-processed with Npn HBTs using the merged process.

The large offset voltage (~1V) observed in the common emitter output characteristics of the Pnp device is not ideal, and is believed to result from a number of factors. The most significant is leakage at the base-collector junction under the base contacts. Because the etch which removes the emitter and stops on the base layer is not as selective on n-GaAs as it is on p-GaAs, the base layer was etched more on the Pnp devices than on the Npn devices. This thinner base layer allowed spiking of the base contact metal (AuGeNi) to penetrate the base-collector junction, providing a source of leakage current. As a result, a bias must be placed on the base-emitter junction to produce a current to offset this excess leakage current. This bias is reflected in the common-emitter offset voltage. Improvements in processing techniques and base layer design should reduce this offset voltage significantly.

RF performance of discrete devices exceeds all other reports to date. Monolithically integrated devices with 1.4 μm x 12 μm emitters show performance levels equal to values typical for separately processed Npn and Pnp transistors. Pnp devices exhibit f_T = 20 GHz and f_{max} = 19 GHz at I_c = -5.5 mA and V_{cc} = -2 V (Fig. 10). Npn devices show f_T = 51 GHz and f_{max} = 60 GHz at I_c = 12 mA and V_{ce} = 1.5 V (Fig. 11). These cutoff frequencies are 2 to 3 times those previously reported for complementary AlGaAs/GaAs HBT processes.[7] The Npn results are typical of our baseline AlGaAs/GaAs HBT structures and process.

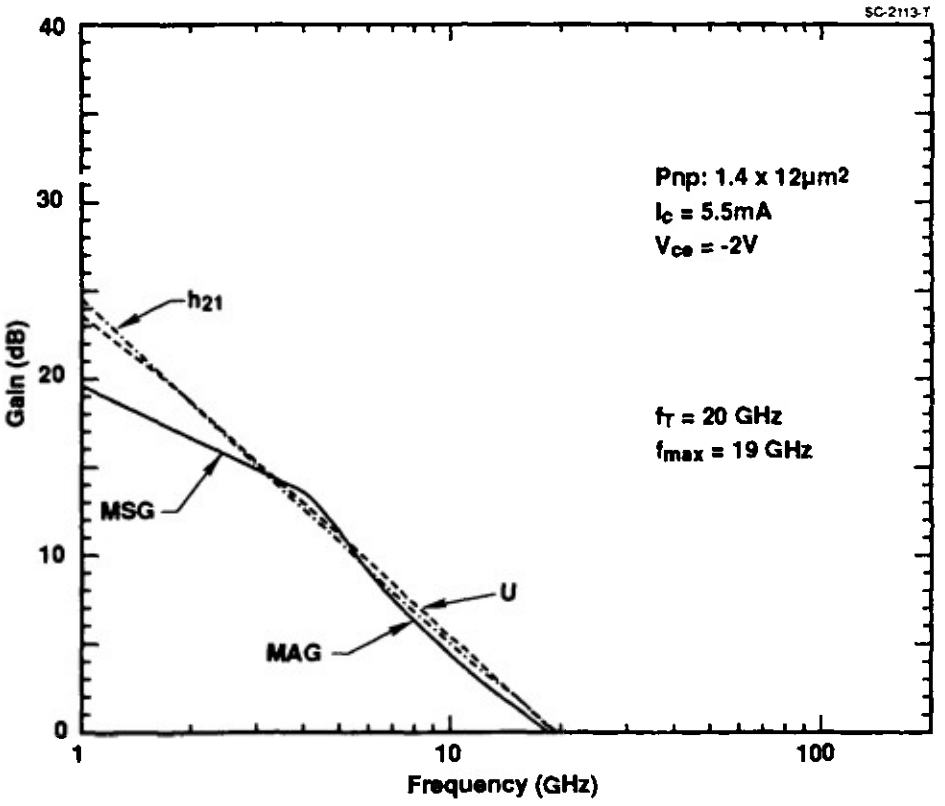


Fig. 10 Pnp rf gain calculated from s-parameters measured up to 20 GHz.

As mentioned previously, edge passivation of the base-emitter junction was used on the Pnp devices for the first time in this program. Edge passivation refers to the retention of AlGaAs on the surface of the device in the area between the base contact metal and the active emitter area. A significant increase in common-emitter current gain was observed in the presence of edge passivation. As shown in Fig. 12, for 70 μm x 70 μm emitter area devices fabricated from a typical Pnp layer structure, the current gain reaches a value of ~6 at a collector current of 10 mA. The same size devices fabricated from the same layer structure with edge passivation show a factor of five increase in gain at 10 mA, as shown in Fig. 13, almost exclusively due to reduction in the excess base current. Because the ideality factor of the base current remains n = 2, which reflects electron-hole recombination in a space charge layer, the excess base current eliminated by edge passivation is believed to come from the space charge layer at the surface of the base layer between the base contact metal and the active emitter area. In addition to reducing unwanted base current, edge passivation also appears to improve the uniformity of the device characteristics, as can be seen from a comparison of Figs. 12 and 13.

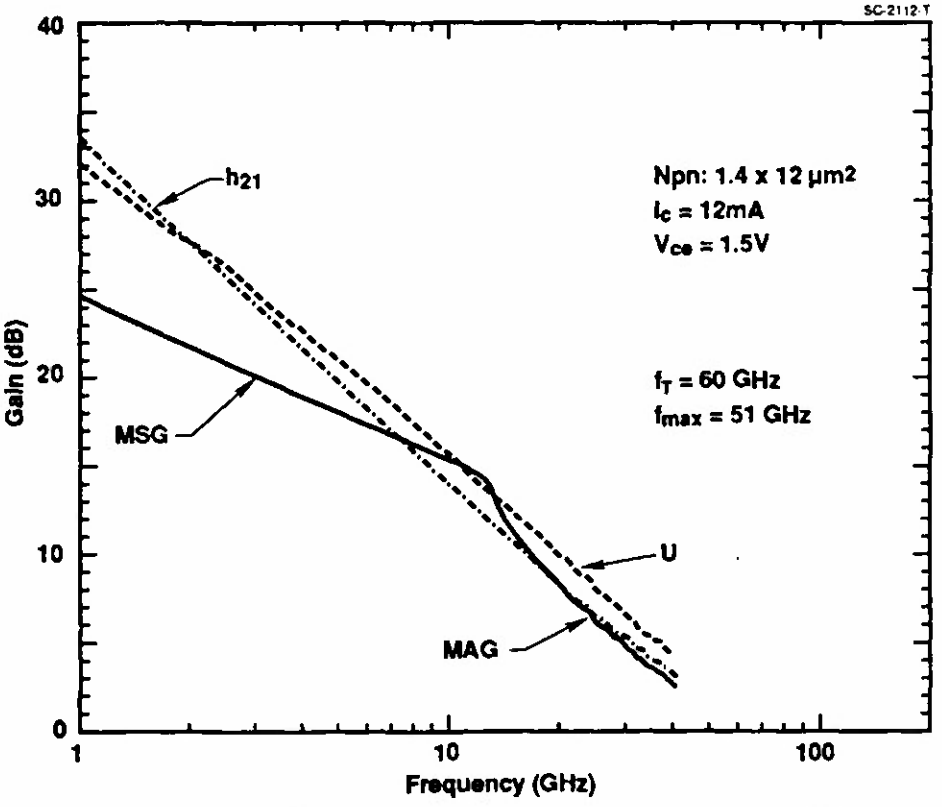


Fig. 11 Npn rf gain calculated from s-parameters measured up to 40 GHz.

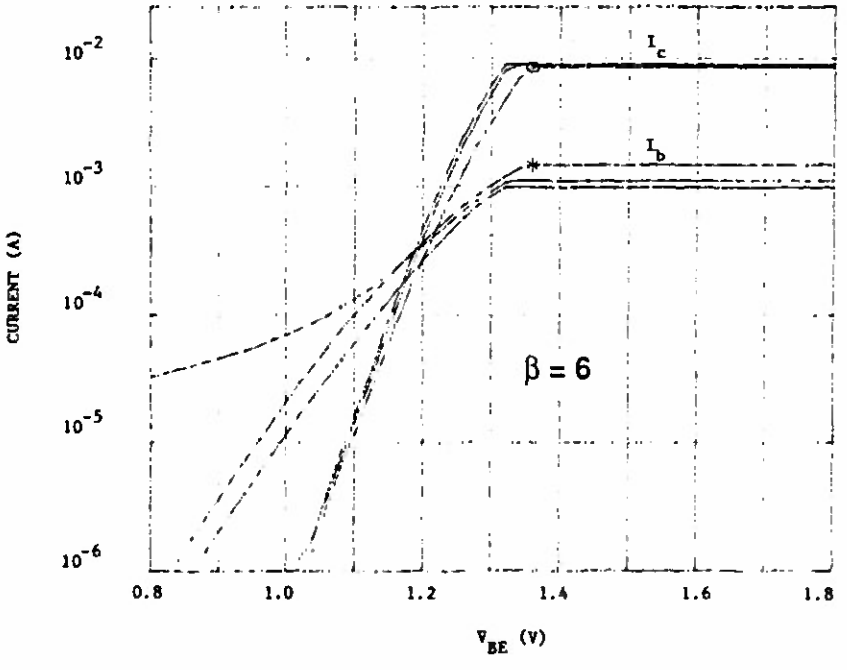


Fig. 12 Gummel plot of AlGaAs/GaAs Pnp HBT without edge passivation.

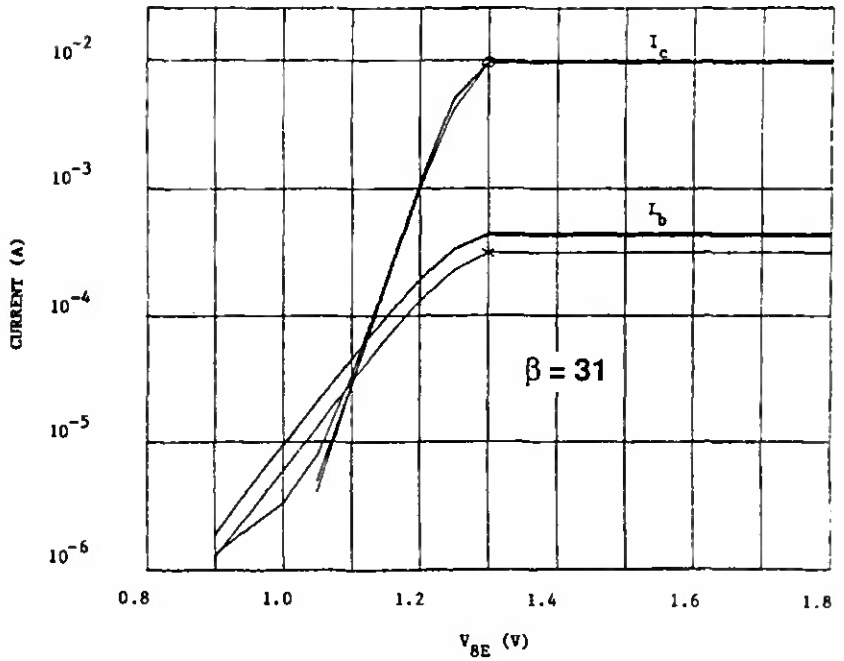


Fig. 13 Gummel plot of AlGaAs/GaAs Pnp HBT with edge passivation.

Integrated circuits have been fabricated from both Npn and Pnp devices monolithically integrated on the same wafer using the merged process. Npn-based direct coupled feedback amplifiers (see circuit schematic in Fig. 14) show a gain of 11 dB and a bandwidth of 12 GHz (Fig. 15). Pnp-based gain blocks show gain of 8 dB and a bandwidth of 6 GHz (Fig. 16). This is the first report of a Pnp-based HBT integrated circuit. This is also the first report of the fabrication of both Npn and Pnp-based microwave frequency ICs on the same wafer.

Significant improvement in Pnp performance can be realized through reduction in emitter resistance, optimized collector layer structures, and higher base doping. Our Pnp cutoff frequencies (f_T = 20 GHz and f_{max} = 19 GHz) are significantly limited by series resistance at the Ti/Pt/Au emitter contact (~30Ω). Alloying experiments on test devices in which the time and temperature of the contact alloy cycle were varied have shown that optimization of the emitter contact alloy cycle can reduce this series resistance by at least a factor of 2. $In_{0.5}Ga_{0.5}As$ contact structures have been examined and result in an additional 5 x reduction in specific contact resistance, which would lead to improvements in both f_T and f_{max}.

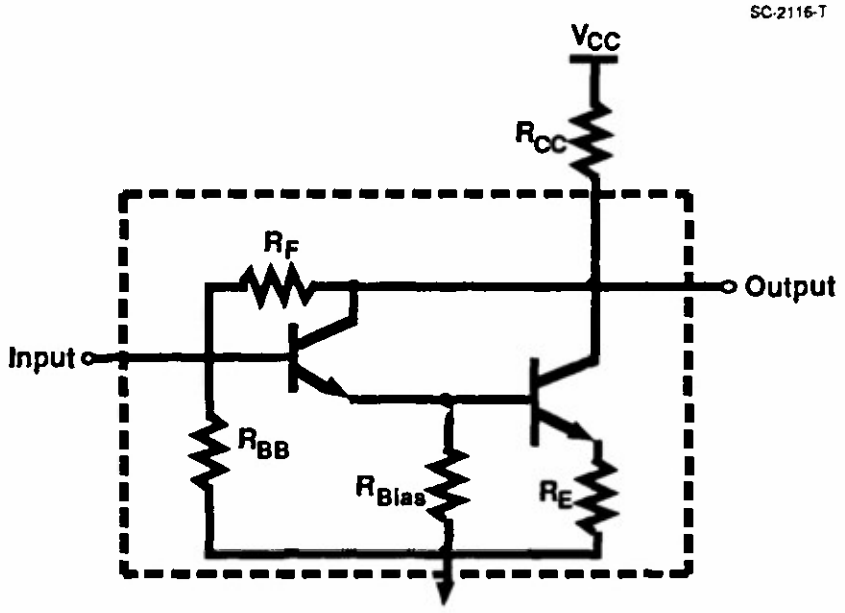


Fig. 14 Schematic of the direct coupled feedback amplifiers fabricated from co-processed HBTs (both Npn and Pnp).

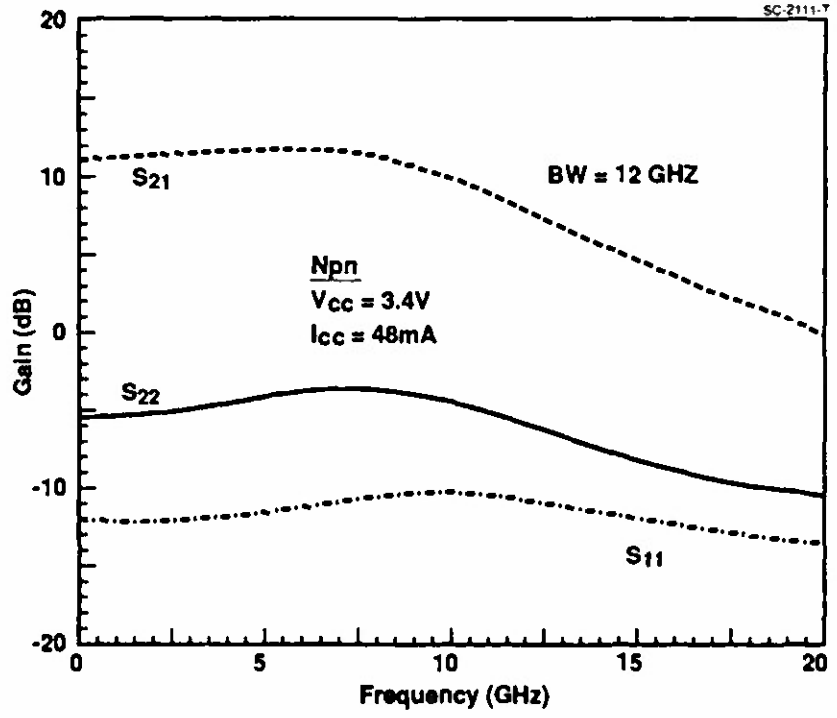


Fig. 15 S-parameter measurements of Npn gain block showing a bandwidth of 12 GHz and low input reflection.

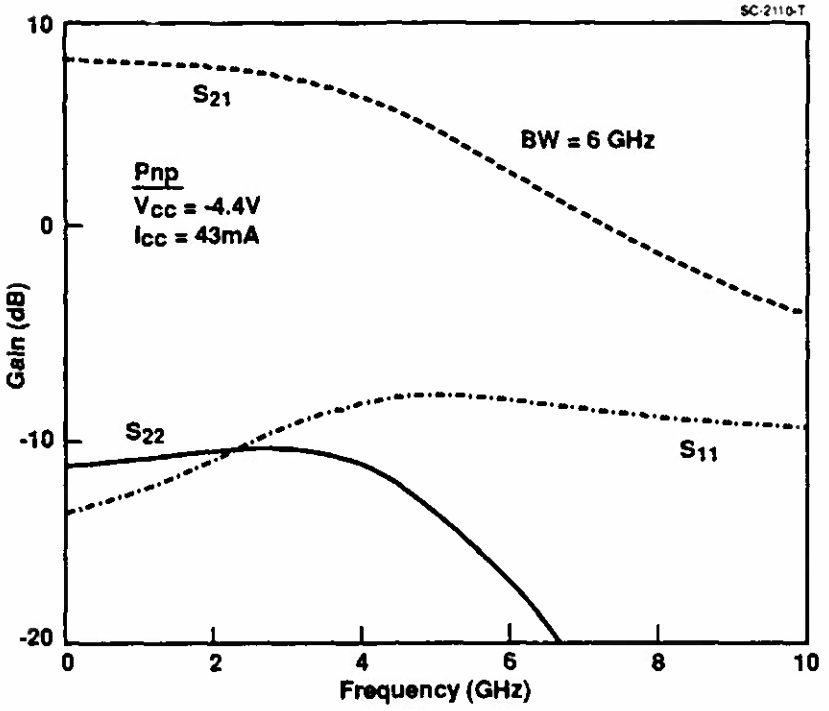


Fig. 16 S-parameter measurements of Pnp gain block showing a bandwidth of 6 GHz and low input reflection.

The absence of any evidence of base-collector breakdown at -5 V for Pnp devices suggests that even thinner collector layers could be used while retaining useful power handling capability; this would lead to shorter collector space charge layer transit times and higher f_T.

Reducing the extrinsic base resistance has already been shown to produce devices with f_{max} as high as 39 GHz.[8] A reasonable expectation is that additional improvements could lead to devices with f_T and f_{max} above 40 GHz, approaching the performance of baseline Npn devices.

Improved device performance should result in improved circuit performance. Direct coupled feedback amplifiers (gain blocks) have been fabricated from Npn and Pnp devices on the same wafer using the merged process, and for the gain blocks, bandwidth (BW) tracks f_{max} (see Fig. 17). For the devices reported here BW ~ 0.3 * f_{max}, demonstrating that Pnp devices can be readily introduced into direct coupled circuit topologies, and that improvements in f_{max} will result in higher circuit operating frequencies, exceeding 10 GHz.

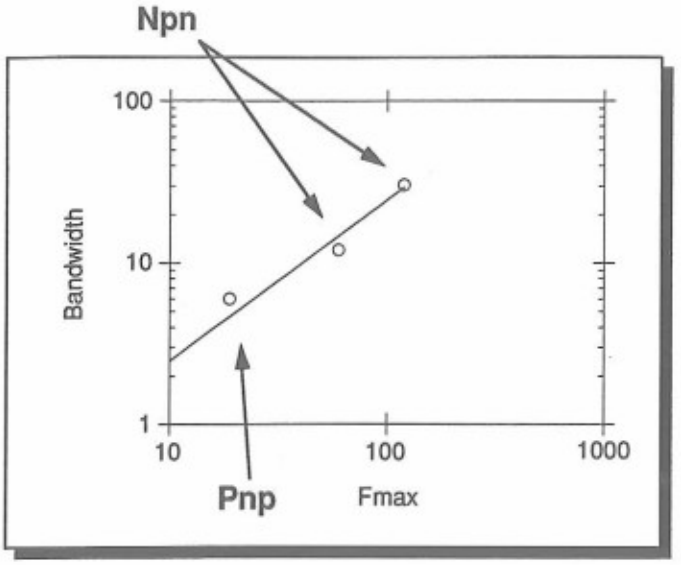


Fig. 17 Comparison of gain block bandwidth and discrete device unity power gain frequency (f_{max}) showing that circuit performance is limited by the power-gain bandwidth of the slowest device.

G. Complementary Circuit Design and Layout

A significant portion of the activity near the end of this program focused on work necessary for implementation of complementary circuits. Modeling of the discrete device characteristics forms the basis for circuit design and performance modeling. Npn devices are well characterized, and since merged processing produced Npn devices with the same characteristics and performance as baseline device structures, existing models were used for circuit design. Discrete device modeling focused on 1.4 μm x 3 μm emitter area Pnp devices. The standard SPICE transistor model was used (parameter values are shown in Fig. 18), with values of emitter, collector, and base resistance calculated from measured sheet resistance on device layers. Ideality factors were extracted from Gummel plots of measured devices. BF and BR were chosen for convenience to be 1000. For other parameters, values applicable to Npn devices were used as a starting point, and modifications were made to produce the best fit to measured common-emitter device characteristics. The results of the SPICE modeling effort using the parameters in Fig. 18 is compared with measured device characteristics in Fig. 19.

BF	1000
BR	1000
RE (OHM)	60
RB (OHM)	1675
RB (OHM)	86
TF (PS)	7
TR (PS)	350
CJE (fF)	9.5
PC (V)	1.4
IS (1.E-23 A)	4.26
NF	1.2
NC	2.0
ISC (1.E-8)	5.26
ISE (1.E-15)	5.0
NE	2.24
EG (V)	1.52
XTI	3.8
XTB	.76
MJE	.5
MJC	.33
CJC (fF)	12.9

Notes: 1. Emitter Area is 1.4μm x 3μm

2. BF and BR are artifically chosen for convenience.

Fig. 18 Spice parameter values for Pnp transistor fabricated using the merged process.

Push-pull amplifiers, as well as a number of digital circuits,were designed. Ring oscillator circuits were designed with variants using Schottky diodes to clamp the base-collector voltage, and prevent the Npn and/or Pnp devices from being driven into saturation. A typical ring oscillator design layout is shown in Fig. 20. A number of logic circuits were designed using Pnp devices as active loads. A typical active load circuit is a CML inverter. Its circuit schematic is shown in Fig. 21. The design layout for this inverter is shown in Fig. 22. Analog circuits, including a push-pull amplifier whose circuit schematic is shown in Fig. 23, were also designed. The design layout for this amplifier is shown in Fig. 24. These and other circuits were laid out on a mask set. The program ended before this mask set was fabricated.

The credibility of complementary HBT integrated injection logic (CHI^2L) technology has been established by the recent demonstration of a seventeen-stage complementary ring oscillator.[9]

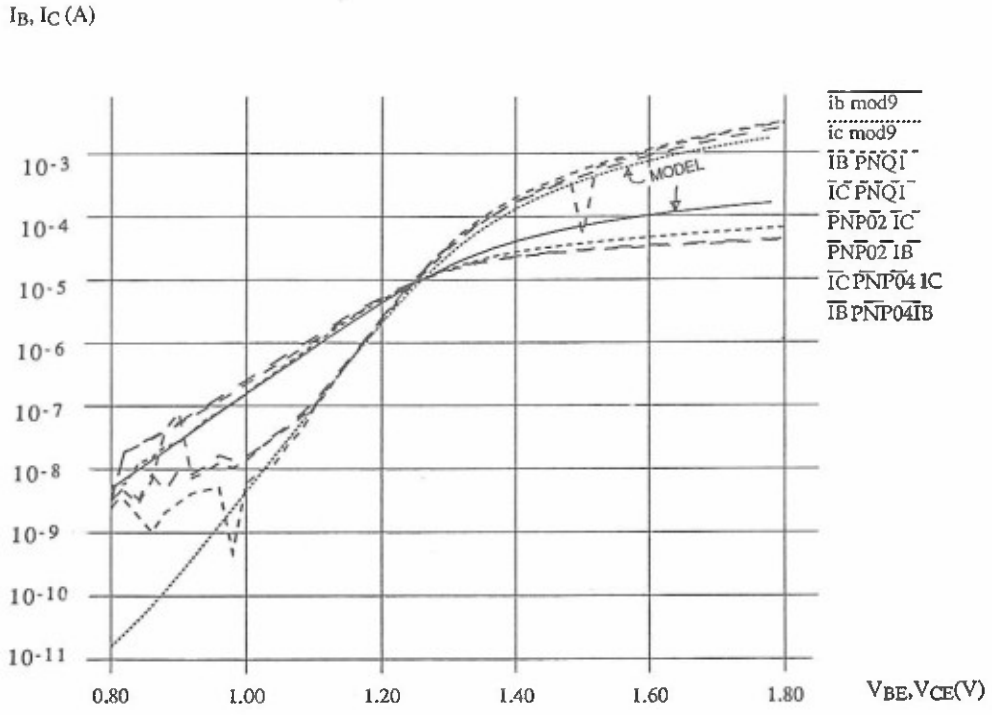


Fig. 19 Spice calculations of common-emitter Pnp device characteristics and comparison with measured characteristics.

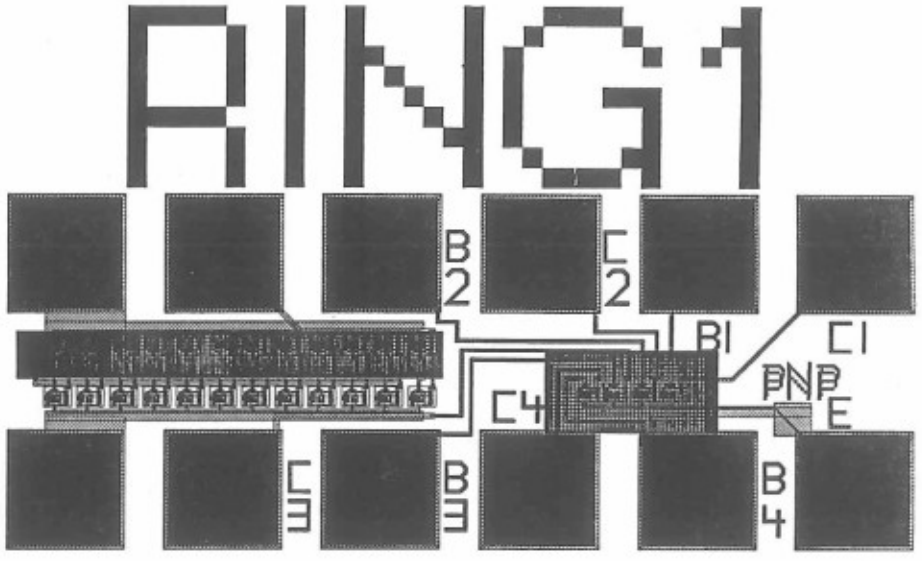


Fig. 20 Design layout for an Npn/Pnp ring oscillator using Schottky clamps on Npn devices to prevent saturation.

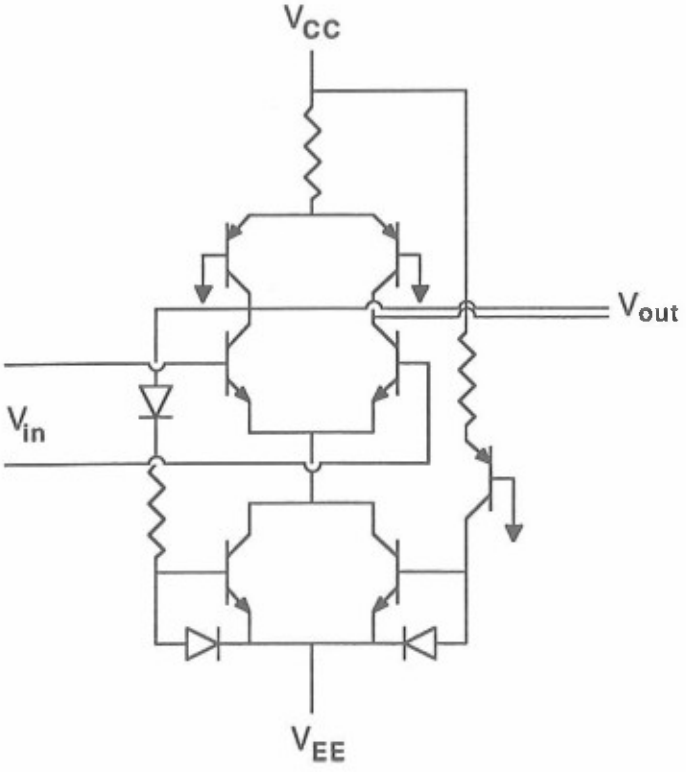


Fig. 21 Circuit schematic of a CML inverter stage using Pnp transistors in place of resistive loads.

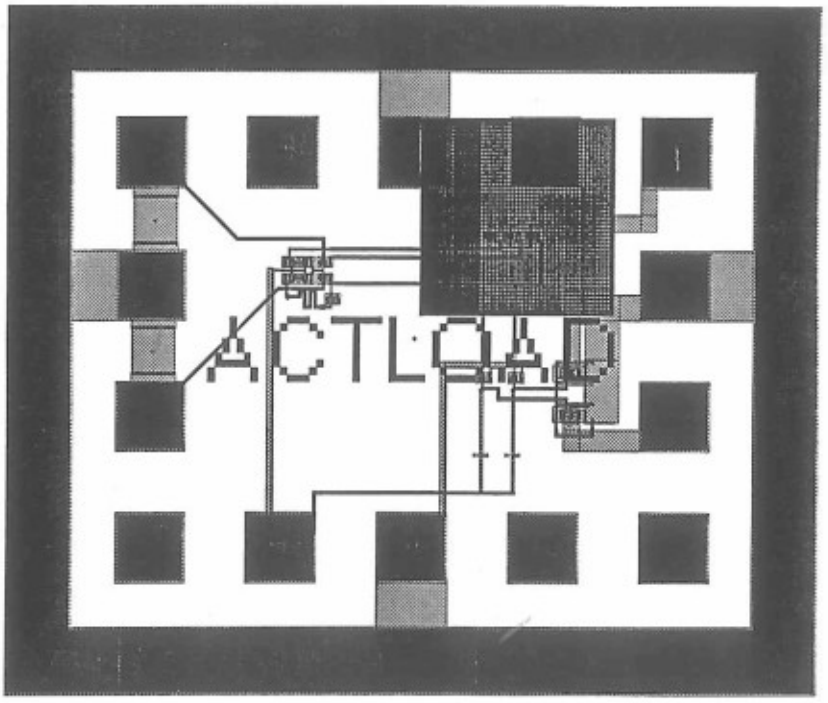


Fig. 22 Design layout for a CML inverter active load demonstration circuit.

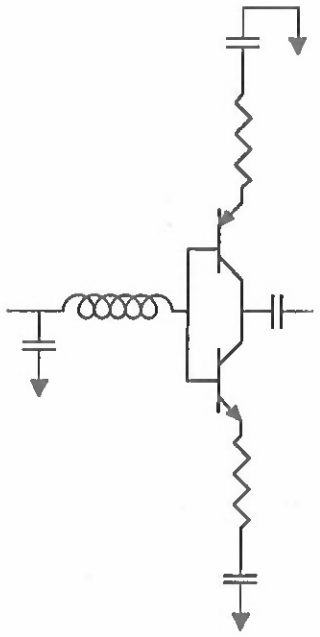


Fig. 23 Circuit schematic of a push-pull complementary power amplifier.

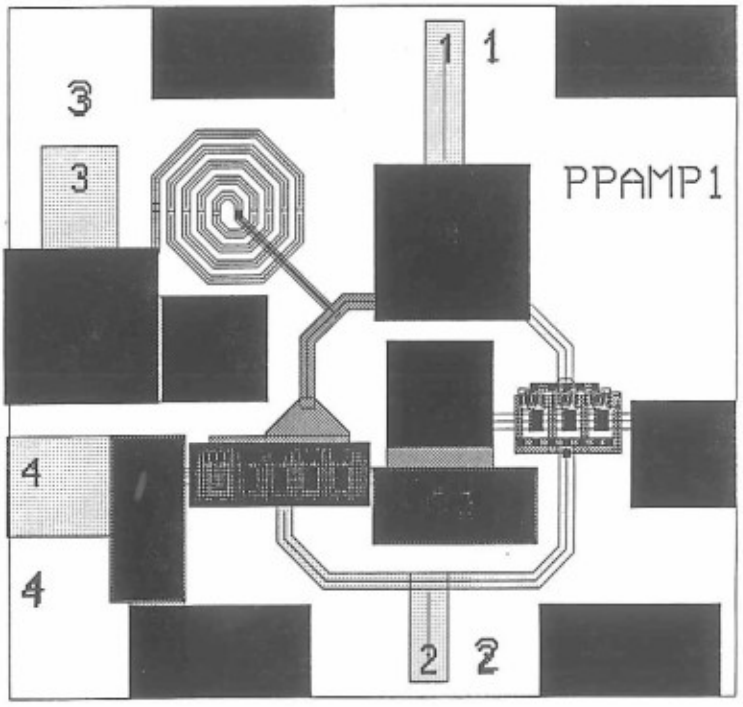


Fig. 24 Design layout of the complementary push-pull amplifier shown in schematic in Fig. 23.

III. LIST OF PUBLICATIONS AND TECHNICAL REPORTS

1. C.W. Farley, R.J. Anderson, R.B. Bernescut, R.W. Grant, M.F. Chang, K.C. Wang, R.B. Nubling, and N.H. Sheng, "High Speed AlGaAs/GaAs Complementary HBT Technology Realized by Multiple MBE Growth and Merged Processing," 1991 IEDM Technical Digest, pp. 927-930.

IV. LIST OF PARTICIPATING SCIENTIFIC PERSONNEL

Dr. C.W. Farley, Principal Investigator

Dr. G.J. Sullivan

R.J. Anderson

R.B. Bernescut

Dr. R.W. Grant

Dr. M.F. Chang

Dr. K.C. Wang

R.B. Nubling

Dr. N.H. Sheng

V. REPORT OF INVENTIONS

Disclosure: "A process for the merged fabrication of complementary HBT devices and circuits".

VI. BIBLIOGRAPHY

1. K. Runge, R.D. Standley, D. Daniel, J.L. Gimlett, R.B. Nubling, R.L. Pierson, S. Beccue, K.C. Wang, N.H. Sheng, M.F. Chang, D.M. Chen, and P.M. Asbeck, "AlGaAs/GaAs HBT ICs for High Speed Lightwave Transmission Systems," to be published in IEEE J. of Solid-State Circuits, Oct. 1992.

2. K. Runge, J.L. Gimlett, R.B. Nubling, K.C. Wang, M.F. Chang, R.L. Pierson, and P.M. Asbeck, "20 Gbit/s AlGaAs/GaAs HBT Decision Circuit IC," Elec. Letters, Vol. 27, No. 25, Dec. 1991, pp. 2376-2378.

3. J.D. George et al., "A High-Speed Gate Array Implemented with AlGaAs/GaAs Heterojunction Bipolar Transistors," ISSCC Dig. Tech. Papers, 1989, pp. 186-187.

4. K.C. Wang et al., "A 15-GHz Gate Array Implemented with AlGaAs/GaAs Heterojunction Bipolar Transistors," IEEE J. of Sol. Sta. Cir., Vol. 26, No. 11, November 1991, pp. 1669-1672.

5. R.B. Nubling, N.H. Sheng, K.C. Wang, M.F. Chang, W.J. Ho, G.J. Sullivan, C.W. Farley, and P.M. Asbeck, "25 GHz HBT Frequency Dividers," Tech. Dig. 1989 GaAs IC Symp., pp. 125-128.

6. M.F. Chang, P.M. Asbeck, K.C. Wang, G.J. Sullivan, N.H. Sheng, J.A. Higgins, and D.L. Miller, "AlGaAs/GaAs Heterojunction Bipolar Transistors Fabricated Using a Fully Self-Aligned Dual-Lift-Off Process," IEEE Elect. Dev. Lett., pp. 303-305, July 1987.

7. D.K. Umemoto, J.R. Velebir, K.W. Kobayashi, A.K. Oki, and D.C. Streit, "Integrated Complementary NPN/PNP Heterojunction Bipolar Transistors Grown by Selective Molecular Beam Epitaxy," to be published in IEEE Electron Device Letters.

8. G.J. Sullivan, M.F. Chang, N.H. Sheng, R.J. Anderson, N.L. Wang, K.C. Wang, J.A. Higgins, and P.M. Asbeck, "AlGaAs/GaAs Pnp HBTs with High f_{max} and f_T," IEEE Electron. Dev. Lett., 11, 463-465 (1990).

9. P.M. Enquist, D.B. Slater, Jr., and J.W. Swart, "Complementary AlGaAs/GaAs HBT I^2L (CHI^2L) Technology," IEEE Electron. Dev. Lett., 13, 180-182 (1992).

APPENDIX I. PUBLICATIONS

High Speed AlGaAs/GaAs Complementary HBT Technology Realized by Multiple MBE Growth and Merged Processing

C.W. Farley, R.J. Anderson, R.B. Bernescut, R.W. Grant, M.F. Chang, K.C. Wang, R.B. Nubling, and N.H. Sheng

Rockwell International Science Center, Thousand Oaks, CA 91360

Abstract

A high performance monolithic Npn/Pnp complementary HBT technology involving multiple MBE growths has been developed. Many of the process steps have been merged to simplify concurrent fabrication of Npn and Pnp devices. Pnp devices exhibit f_T=20 GHz and f_{max}=19 GHz. Npn devices show f_T=51 GHz and f_{max}=60 GHz. These cutoff frequencies are 2 to 3 times values previously reported for monolithically integrated Npn and Pnp devices. For the first time, integrated circuits operating at microwave frequencies have been fabricated from both types of devices on the same wafer. Npn-based direct coupled feedback amplifiers (gain blocks) show a gain of 11dB and a 3 dB bandwidth of 12 GHz. Pnp-based gain blocks show a gain of 8dB and a 3 dB bandwidth of 6 GHz.

Introduction

With the transfer of baseline Npn AlGaAs/GaAs heterojunction bipolar transistor (HBT) technology into integrated circuit (IC) production, more attention has been given to exploration of the potential applications of HBT device technology [1]. The attractiveness of complementary HBT circuits for both analog and digital applications has led to the development of Pnp AlGaAs/GaAs HBTs with f_T as high as 19 GHz and f_{max} as high as 39 GHz [2], with further improvement in device performance to be expected. Because of the large difference in electron and hole mobilities, the optimal layer structures for Npn and Pnp devices are very different [3]. Realizing the full potential of Pnp devices, especially in complementary circuits, will require optimized epitaxial layer design and flexible processing techniques to accommodate the differences in Npn and Pnp layer structure.

There are a number of applications for Pnp devices in complementary Npn/Pnp circuits. For example, Pnp transistors can be used as active loads in the feedback path of operational amplifiers, greatly improving amplifier gain at frequencies above 1 GHz. Complementary push-pull amplifiers can be fabricated which have the potential for very high linearity and high output power levels at frequencies approaching 10 GHz. In addition, complementary HBT logic (CHBTL) can be realized, which could lead to a high speed logic family with reduced standby power dissipation. This would relax some of the thermal constraints on the integration level achievable with HBTs and expand the range of potential applications. Several milestones in the development of complementary technology have already been achieved. Complementary circuits operating at low frequency (DC) have been fabricated with selective MOVPE [4]. Microwave frequency Npn and Pnp transistors have been fabricated on the same wafer using selective MBE growth and merged processing, however, the device structures were compromised to accommodate processing constraints, which resulted in reduced frequency response [5].

In this paper, we report the concurrent fabrication of microwave frequency complementary HBTs in which no compromises in either Npn or Pnp device performance were made to accommodate process constraints. As a result, we have fabricated devices with cutoff frequencies 2 to 3 times higher than those previously reported for monolithically integrated Npn and Pnp transistors [5]. In addition, we report the first characterization of functional high speed Npn and Pnp HBT ICs fabricated on the same wafer concurrently with the discrete devices.

Experimental Procedures

The devices and circuits whose performance is described below were fabricated from Npn and Pnp layer structures (shown in Fig. 1) which had been developed and optimized separately. The Npn device structure is identical to the structure used for the commercial manufacturing of ICs. The process has been designed to use refractory metallization throughout, to simplify the transfer of complementary HBT technology from research to production. The device structures used were conservatively designed, but were not modified to accommodate processing constraints. Rather, process refinements were developed to accommodate the more stringent requirements of merged processing of Npn and Pnp HBTs. Because of concern over Be diffusion

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during Npn regrowth, the Pnp emitter and collector contact layers were only doped to 5×10^{19} cm^{-3}. Optimization of these contact layers would lead to further improvement in device bandwidth.

The complementary process begins with the growth of the Pnp transistor. A dielectric stack of SiO_2/Si_3N_4 is used to protect the Pnp layers so that they can be selectively removed in regions where Npn devices will be located. In the second MBE growth, Npn device layers are grown in these wells. The polycrystalline overgrowth on the dielectric is removed over the Pnps, followed by removal of the dielectric. This process results in good morphology within 3-5 microns of the boundary between device types. Experiments involving a thermal cycle to simulate the Npn regrowth show that there is no degradation in Pnp device characteristics (gain or turn-on voltage) as a result of the Npn regrowth. Both Npn and Pnp devices are processed simultaneously (on a field-by-field basis) in this work. The merged process requires only 4 additional mask levels.

Device performance

DC results are presented for small (1.4 μm x 3 μm emitter) devices. Npn devices show a maximum value of β=200 at I_c=4 mA and V_{ce}=1.3 V. Pnp devices show a maximum value of β=140 at I_c=-2.5 mA and V_{ce}=-2.2 V. The gain in these devices is significantly higher than that reported previously for devices on the same wafer [4,5], and reflects the absence of compromises in layer structure design. The Npn common-emitter characteristics are shown in Figure 2(a). Nearly ideal device behavior is observed, with low offset voltage, low output conductance, and current gain which is relatively independent of operating current. The Pnp common-emitter characteristics are shown in Figure 2(b). These devices show a high series resistance (~120Ω) resulting from the use of both a refractory metal contact to an emitter contact layer with moderate doping and a standard alloy cycle. This series resistance also contributes to a stronger dependence of gain on collector current than is observed for Npn devices. Such bias dependence is typical of Pnp devices reported to date [2,4,5]. Experiments on test devices have shown that optimization of the emitter contact alloy cycle can reduce this series resistance by at least a factor of 2. $In_{0.5}Ga_{0.5}As$ contact structures have been examined and result in an additional 5 x reduction in specific contact resistance.

Microwave performance of discrete devices exceeds all other reports to date. Monolithically integrated devices with 1.4 μm x 12 μm emitter fingers show performance levels equal to separately processed Npn and Pnp transistors. As shown in Figure 2(c), Npn devices show f_T=51 GHz and f_{max}=60 GHz at I_c=12 mA and V_{ce}=1.5 V. The Npn results are typical of our baseline AlGaAs/GaAs HBT structures and process, and reflect the performance level achievable using a layer structure and process compatible with the manufacturing of HBT ICs. As shown in Figure 2(d), Pnp devices exhibit f_T=20 GHz and f_{max}=19 GHz at I_c=-5.5 mA and V_{ce}=-2 V. The Pnp cutoff frequencies are significantly limited by series resistance at the Ti/Pt/Au emitter contact (~30Ω). As mentioned above, this series resistance can be reduced by as much as a factor of ten, which would lead to improvements in both f_T and f_{max}. The absence of any evidence of base-collector breakdown at -5 V suggests that even thinner collector layers could be used while retaining useful power handling capability; this would lead to shorter collector space charge layer transit times and higher f_T. Reducing the extrinsic base resistance by increasing the base doping to 7×10^{18} cm^{-3} has already been shown to produce devices with f_{max} as high as 39 GHz [2]. A reasonable expectation is that these improvements could lead to devices with f_T and f_{max} above 40 GHz, approaching the performance of baseline Npn devices. Both Npn and Pnp devices operate up to frequencies 2 to 3 times higher than those previously reported for complementary AlGaAs/GaAs HBT processes [4,5].

Direct coupled feedback amplifiers (gain blocks) have been fabricated from both types of devices on the same wafer using the merged process. The design and demonstration of these circuits are discussed elsewhere [6]. The circuit schematic for the Npn gain block is shown in Figure 3(a). Shown in Figure 3(b) is the measured transmission power gain (S_{21}), as well as the input and output power reflection (S_{11} and S_{22}) as a function of frequency. Npn-based gain blocks show a gain of 11dB and a 3 dB bandwidth of 12 GHz. The circuit schematic for the Pnp gain block is shown in Figure 4(a). As shown in Figure 4(b), where transmission power gain as well as input and output power reflection are plotted, Pnp-based gain blocks show a gain of 8dB and a 3 dB bandwidth of 6 GHz. This is the first report of a Pnp-based HBT integrated circuit operating at microwave frequencies. This is also the first report of the merged fabrication of both Npn- and Pnp-based ICs on the same wafer. The bandwidth of these gain blocks largely reflects the maximum operating frequencies of the Npn and Pnp devices. For Npn AlGaAs/GaAs HBTs, gain block 3dB bandwidths as high as 30.5 GHz have been observed for devices fabricated using a fully self-aligned process, yielding f_T=60 GHz and f_{max}=120 GHz [6]. Bandwidth tracks f_{max} for the devices reported here ($BW = 0.3 \times f_{max}$), demonstrating that Pnp devices can be readily introduced into direct coupled circuit topologies.

Summary

A high performance monolithic Npn/Pnp complementary HBT technology involving two MBE growths and merged processing has been achieved. This process was developed with device structures separately optimized for performance. Devices have been fabricated with cutoff frequencies which are 2 to 3 times higher than values previously reported. Further development of the Pnp structure and process should lead to cutoff frequencies approaching 40 GHz. For the first time, ICs operating at high frequency have been fabricated from both types of devices on the same wafer using a merged process. Npn-based gain blocks show a gain of 11dB and a 3 dB bandwidth of 12 GHz. Pnp-based gain blocks show a gain of 8dB and a 3 dB bandwidth of 6 GHz. The device process reported here has the potential to realize high linearity, high efficiency Class B push-pull amplifiers, operational amplifiers, and low static power complementary logic circuits operating at frequencies approaching 10 GHz.

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References

1. P.M. Asbeck, M.F. Chang, J.A. Higgins, N.H. Sheng, G.J. Sullivan, K.C. Wang, "GaAlAs/GaAs Heterojunction Bipolar Transistors: Issues and Prospects for Application", IEEE Trans. Electron Devices, Vol. 36, No. 10, p. 2032, Oct. 1989.

2. G.J. Sullivan, M.F. Chang, N.H. Sheng, R.J. Anderson, N.L. Wang, K.C. Wang, J. A. Higgins, and P.M. Asbeck, "AlGaAs/GaAs P-n-p HBTs with High Maximum Frequency of Oscillation", IEEE Electron Device Letters, Vol. 11, No. 10, p. 463, October 1990.

3. D.A. Sunderland and P.D. Dapkus, "Optimizing N-p-n and P-n-p Heterojunction Bipolar Transistors for Speed", IEEE Trans. Electron Devices, Vol. ED-34, No. 2, p. 367, February 1987.

4. D.B. Slater, P.M. Enquist, F.E. Najiar, M.Y. Chen, and J.A. Hutchby, "Monolithic Integration of Complementary HBTs by Selective MOVPE", IEEE Electron Device Letters, Vol. 11, No. 4, p. 146, April 1990.

5. D.K. Umemoto, J.R. Velebir, K.W. Kobayashi, A.K. Oki, and D.C. Streit, "Integrated Complementary NPN/PNP Heterojunction Bipolar Transistors Grown by Selective Molecular Beam Epitaxy", to be published in IEEE Electron Device Letters.

6. N.H. Sheng, W.J. Ho, N.L. Wang, R.L. Pierson, P.M. Asbeck, and W.L. Edwards, "A 30 GHz Bandwidth AlGaAs/GaAs HBT Direct-Coupled Feedback Amplifier", to be published in Microwave and Guided Wave Letters, August 1991.

Npn Layer Structure

Contact	InAs	$n=1 \times 10^{20}$	600Å
n^+ Cap	GaAs	$n=1 \times 10^{18}$	1000Å
Emitter	AlGaAs	$n=5 \times 10^{17}$	950Å
Base	GaAs	$p=4 \times 10^{19}$	800Å
Collector	GaAs	$n=3.6 \times 10^{16}$	7000Å
Subcollector	GaAs	$n=6 \times 10^{18}$	6000Å
Substrate	GaAs	undoped	25 mils

Pnp Layer Structure

Contact	GaAs	$p=5 \times 10^{19}$	500Å
n^+ Cap	GaAs	$p=1 \times 10^{19}$	1000Å
Emitter	AlGaAs	$p=5 \times 10^{17}$	950Å
Base	GaAs	$n=1.4 \times 10^{18}$	800Å
Collector	GaAs	$p=4 \times 10^{16}$	4000Å
Subcollector	GaAs	$p=4 \times 10^{19}$	8000Å

Figure 1. MBE layer structure cross sections for the devices used in this paper.

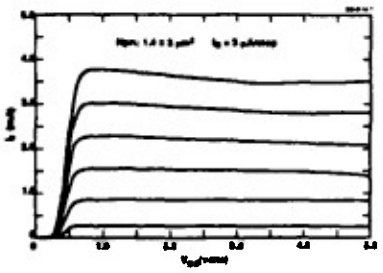
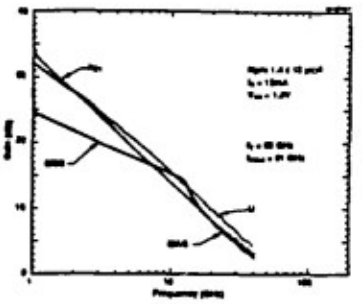
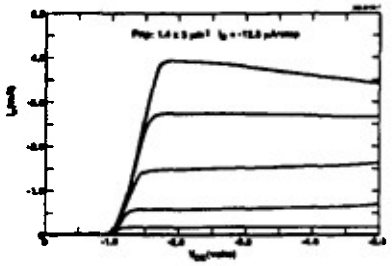


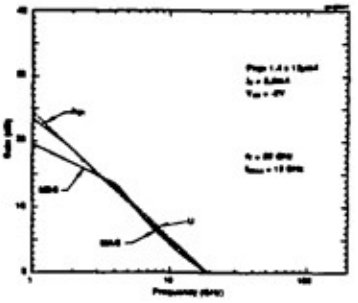
Figure 2. (a) Common-emitter characteristics of a typical Npn device with a 1.4 μm x 3 μm emitter. Base current: 3 μA per step.



(b) Common-emitter characteristics of a typical Pnp device with a 1.4 μm x 3 μm emitter. Base current: -12.5 μA per step.



(c) Microwave current and power gain for a 1.4 μm x 12 μm Npn device extracted from s-parameter measurements. For this device, f_T=51 GHz and f_{max}=60 GHz.



(d) Microwave current and power gain for a 1.4 μm x 12 μm Pnp device extracted from s-parameter measurements. For this device, f_T=20 GHz and f_{max}=19 GHz.

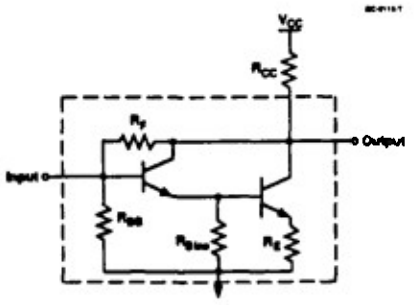
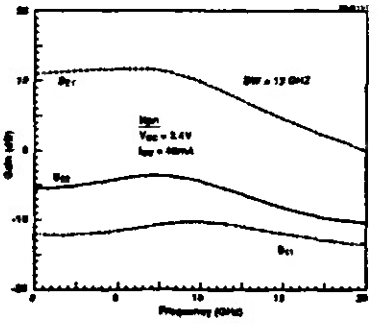


Figure 3. (a) Schematic of the Npn-based direct coupled feedback amplifier (gain block).



(b) Power transmission (S_{21}) and reflection (S_{11},S_{22}) parameters measured for the Npn gain block operating at V_{CC}=3.4 V and I_{CC}=48 mA, showing a 3 dB bandwidth of 12 GHz.

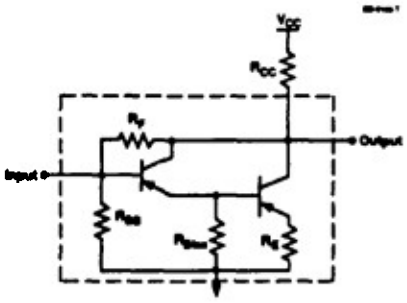
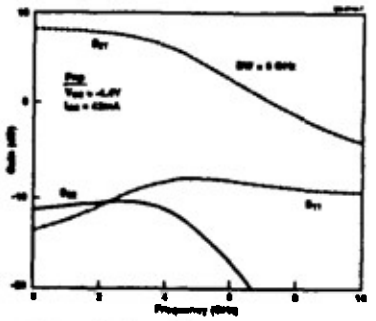


Figure 4. (a) Schematic of the Pnp-based gain block.



(b) Power transmission (S_{21}) and reflection (S_{11},S_{22}) parameters measured for the Pnp gain block operating at V_{CC}=-4.4 V and I_{CC}=-43 mA, showing a 3 dB bandwidth of 6 GHz.